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A Novel Multilevel DC/AC Inverter Based on Three-Level Half Bridge With Voltage Vector Selecting Algorithm

CHAO ZHANG AND ZHIGANG GAO
Beijing Institute of Technology, Beijing 100081, China
Corresponding author: Zhigang Gao (gzgbit@126.com)

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ABSTRACT A novel multilevel inverter based on a three-level half bridge is proposed for the DC/AC applications. For each power cell, only one DC power source is needed and five-level output AC voltage is realized. The inverter consists of two parts, the three-level half bridge, and the voltage vector selector, and each part consists of the four MOSFETs. Both positive and negative voltage levels are generated at the output, thus, no extra H bridges are needed. The switches of the three-level half bridge are connected in series, and the output voltages are (V_o, V_o/2, and 0). The voltage vector selector is used to output minus voltages ($-V_o$ and $-V_o$/2) by different conducting states. With complementary working models, the voltages of the two input capacitors are balanced. Besides, the power cell is able to be cascaded for more voltage levels and for higher power purpose. The control algorithm and two output strategies adopted in the proposed inverter are introduced, and the effectiveness is verified by simulation and experimental results.

INDEX TERMS Bridge circuits, DC-AC power converters, modular multilevel converters, pulse width modulation converters, voltage control.

I. INTRODUCTION

With the development of science and technology, the energy crisis and pollution problems occur. Traditional ways of power generation such as thermal power are the main reason of the air pollution, and the coal heating in the winter leads to smog. However, the traditional energies are not infinite, thus renewable energy harvesting technology shows remarkable aptitude in green power networks and is expected to be pervasively utilized to reduce carbon footprints [1]. Among clean energies, solar energy plays an important role due to its good characteristics. For instance, the implementation of it is much easier and cheaper than wind power and water power. Research on the smart grid is being given enormous supports worldwide due to its great significance in solving environmental and energy crisis [2]. For solar energy, it is usually produced personally, and some of it is consumed personally, while the redundant energy is transformed to AC power and then inject to the power grid. Thus, to improve the power quality of personal energy, DC/AC inverters with lower harmonic distortions and higher power quality are needed.

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Multilevel inverter is a common used inverter worldwide due to its good output characteristics, low THD (Total Harmonic Distortion) performance and low EMI losses. There are already lots of multilevel inverters, among which CHB (cascaded H bridge) inverter plays an important role due to its good output characteristics [3]–[5]. Some control strategies are introduced to eliminate circulation power flow [6] and realize ZVS (zero voltage switch) performance [7]. There are some other multilevel inverters [8]–[14]. A new single-phase cascaded multilevel inverter comprised of a series connection of basic units is proposed in [8], however, only positive levels are generated at the output, thus additional H bridge is needed. A novel multilevel DC/AC inverter is introduced in [9], and a single-stage switched-capacitor module topology for cascade multilevel inverter is introduced in [10]. An optimized three-phase multilevel inverter derived by cascading the level generation part with the phase sequence generation part is introduced in [11], [12]. Three-phase active balance of modular hybrid asymmetrical cascaded multilevel drives are introduced in [13] to solve energy imbalances of the low-voltage cells. A generalized multilevel inverter is introduced in [14], and it can be cascaded as submultilevel inverter using series connection for higher power purpose. PUC5 inverter and T3 inverter are introduced and compared in [15], only one DC source is used in these inverters and less switches and more voltage levels (up to 7 levels) are realized in PUC5 inverter. However, the voltage of the auxiliary capacitor should be controlled in a complex and high frequency method. More switches are needed for 5-level output voltage in T3 inverter, and half of them suffer the whole DC bus voltage. FC inverters are introduced in [16], [17], though more voltage levels are realized, the implementation of large number of flying capacitors leads to large size, high losses and complex voltage control method. Though lots of multilevel inverters have been applied, one with reduced semiconductors and more output voltage levels (which leads to higher output quality with lower THD) is still a challenge.

While some control algorithms and strategies are introduced [18]–[24]. A systematic design of high-performance hybrid cascaded multilevel inverter is introduced on active voltage balance and minimum switching losses with simplified DC power supplies in [18]. Virtual prototyping for distributed control is introduced for fault-tolerant inverters for photovoltaics in [19]. A generalized DTC (direct torque control) strategy is introduced to reduce the torque ripple in multilevel inverters [20]. An analysis on THD is given on single and three phase multilevel inverters [21]. Method to accelerate harmonic minimization by using a parallel genetic algorithm on graphical processing unit is introduced in [22]. A control algorithm to overcome the photovoltaic partial shading is introduced on multilevel DC-link inverter [23]. A reduced switching loss SPWM strategy to eliminate common-mode voltage in multilevel inverters is introduced in [24]. The control algorithm of the topology in this paper takes lots of lessons from these control strategies above.

A novel multilevel inverter based on a three-level half bridge is proposed for DC/AC applications is proposed in this paper. For each power cell, only one DC power source is needed and 5-level output AC voltage is realized. The inverter consists of two parts, the three-level half bridge and the voltage vector selector, and each part consists of four MOSFETs. Both positive and negative levels are generated at the output, thus no additional H bridges are needed. The non-isolated structure eliminates the magnetic losses (normally caused by transformers). The switches of the three-level half bridge are connected in series, and the output voltages are V_o, $V_o/2$, 0. The voltage vector selector is used to output minus voltages ($-V_o$, $-V_o/2$) by different conducting states. With complementary working models and voltage strategy, the voltages of the two input capacitors are balanced. Besides, the cascaded ability is realized for more voltage levels and for higher power purpose. The space vector selecting control algorithm is adopted in the proposed inverter. Besides, both high frequency SPWM (pulse width modulation) control strategy and low frequency fitting strategy are proposed in the inverter for numerous load condition.

This paper is organized as follows, the configuration of the proposed inverter is described in Section II. The working stages and working principle are analyzed in Section III. Two output strategies, the voltage balance strategy as well as the stage optimization method are introduced in Section IV. Simulation and experimental results are given in Section V and Section VI respectively. In the end, the paper is concluded in Section VII.

II. CONFIGURATION OF THE PROPOSED INVERTER

The configuration of the proposed multilevel inverter is shown in Fig. 1. The power supply is a DC voltage source (v_i, a battery for example), and two capacitors (C_1 and C_2) are connected in series on the DC bus. The 3-level half bridge consists of four power switches connected in series (S_1, S_2, S_3, and S_4), and each output point (a or b) has two voltage levels. As for the voltage vector selector, two switches (K_1 and K_2) are connected in series between the output of the 3-level half bridge (a and b), while two switches (Q_1 and Q_2) are connected in series on the DC bus.

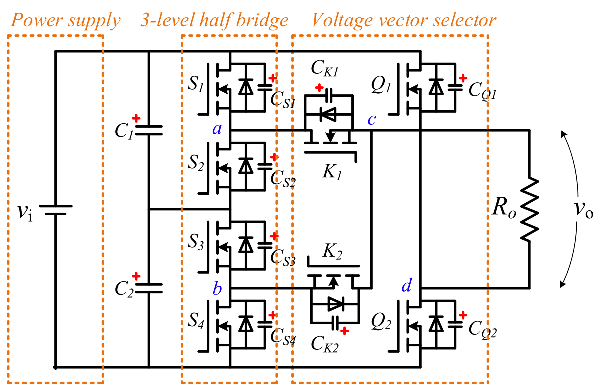

FIGURE 1. The proposed hybrid ZVS bidirectional DC/AC inverter topology.

As shown in Fig. 1, C_{S1}, C_{S2}, C_{S3} and C_{S4} are the parasitic capacitors of the power switches in the 3-level half bridge, while C_{K1}, C_{K2}, C_{Q1} and C_{Q2} are the parasitic capacitors of the switches in the voltage vector selectors. R_o is the resistant load. v_o is the multilevel output voltage.

III. VOLTAGE GENERATION AND WORKING PRINCIPLE

A. VOLTAGE LEVEL ANALYSIS

The voltage levels of point a, b, c, d and the output port are illustrated in Fig. 2.

As shown in Fig. 1, the input voltage v_i is divided into $v_i/2$ on each series connected capacitor (C_1 or C_2). Due to the switching state of S_1-S_4, the voltage of point a and b are shown in Fig. 2, there are two voltage levels on each point. While switches K_1 and K_2 work as a selector, it determines which point (a or b) connected to point c. As a result, three voltage levels are obtained at point c. The switches Q_1 and Q_2 work as another selector to determine the voltage level of point d, and two voltage levels are obtained on this point. Finally, the output voltage is the voltage difference between

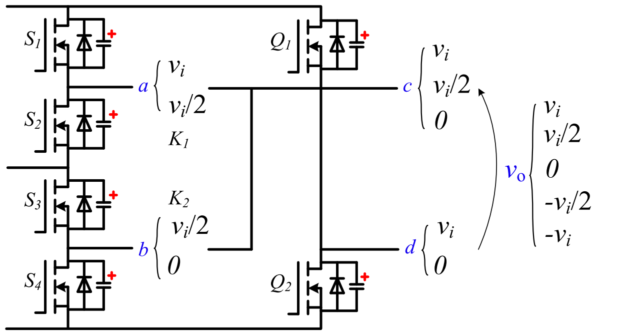

FIGURE 2. Illustration of the voltage levels.

point c and d, due to different chooses of switching state, five voltage levels are realized on the output port.

B. SWITCHING VECTOR ANALYSIS

The switching vectors are shown in Fig. 3.

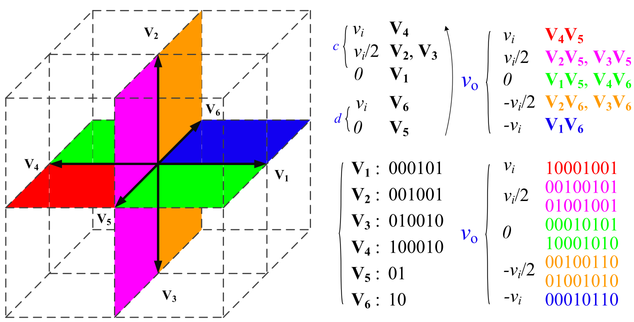

FIGURE 3. Illustration of the voltage vectors and switching states.

As shown in Fig. 3, six vectors are introduced to illustrate the switching states. The switching state of switches S_1-S_4 and K_1-K_2 which determines the voltage level of point c is illustrated from vector $\mathbf{V_1}$ to vector $\mathbf{V_4}$. While the switching state of switches Q_1-Q_2 which determines the voltage level of point d is illustrated form vector $\mathbf{V_5}$ to vector $\mathbf{V_6}$. As shown in the binary sequences in Fig. 3, "1" represents conducting and "0" represents dis-conducting. The switch order of $\mathbf{V_1}$-$\mathbf{V_4}$ is S_1-S_4 & K_1-K_2, and the switch order of $\mathbf{V_5}$-$\mathbf{V_6}$ are Q_1-Q_2. Three voltage levels are realized on point c due to the selection of $\mathbf{V_1}$-$\mathbf{V_4}$ and two voltage levels on point d are realized due to the selection of $\mathbf{V_5}$-$\mathbf{V_6}$. As the output voltage is the voltage difference of point c and point d. Different combinations between $\mathbf{V_1}$-$\mathbf{V_4}$ and $\mathbf{V_5}$-$\mathbf{V_6}$ lead to different output voltages. As shown in Fig. 3, $\mathbf{V_1}$ and $\mathbf{V_4}$, $\mathbf{V_2}$ and $\mathbf{V_3}$ as well as $\mathbf{V_5}$ and $\mathbf{V_6}$ are on the exact complimentary switching states, thus the vectors are in the opposite directions. While $\mathbf{V_1}$-$\mathbf{V_4}$ which determines the voltage level of point c are in the same plane, $\mathbf{V_5}$-$\mathbf{V_6}$ which determines the voltage level of point d are in the vertical plane. The voltage level selections of point c and point d are independent and uncorrelated. Besides, the output voltage levels are distinguished in different colors in Fig. 3, red for v_i, pink for $v_i/2$, green for 0, yellow for $-v_i/2$ and blue for $-v_i$.

C. EQUIVALENT CIRCUITS AND WORKING STAGES ANALYSIS

Fig. 4-11 show the equivalent circuits of all working stages. There are three half bridges in the proposed inverter, the first one is the 3-level half bridge consisting of switches S_1-S_4, the second one is former part of the voltage selector consisting of switches K_1-K_2, and the last one is the latter part of the voltage selector consisting of switches Q_1-Q_2. It is illustrated that there is only one switch conducting in each half bridge during any working stage.

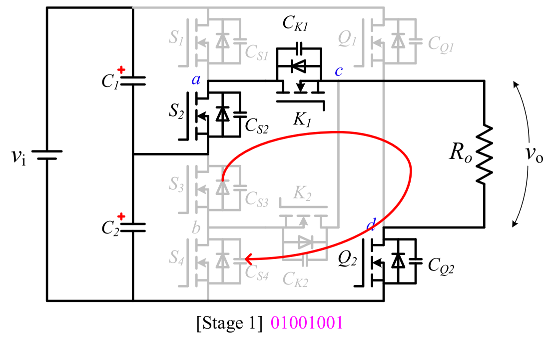

FIGURE 4. Equivalent circuits of [Stage 1].

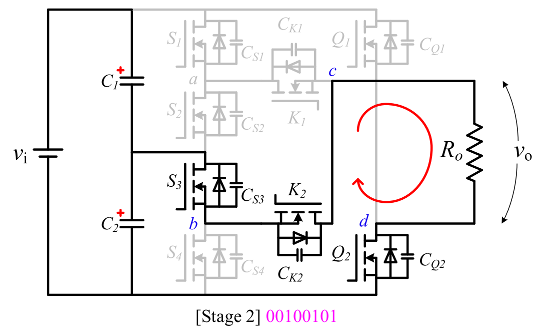

FIGURE 5. Equivalent circuits of [Stage 2].

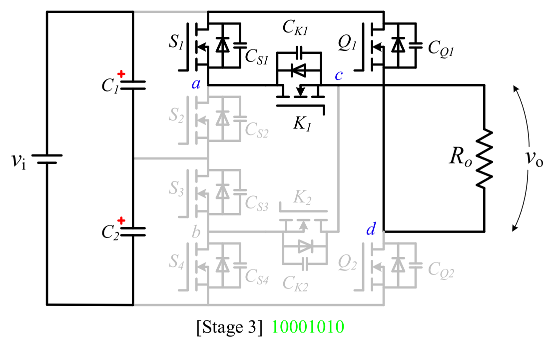

FIGURE 6. Equivalent circuits of [Stage 3].

[Stage 1] (01001001): While S_2, K_1 and Q_2 are conducting in this stage, input capacitor C_2 is connected to the load. Thus the output voltage is clamped to $v_i/2$. The input capacitor C_2 is discharged in this stage, while the input capacitor C_1 is charged by the input voltage source at the same time, as a result the voltage sum of C_1 and C_2 keeps the same.

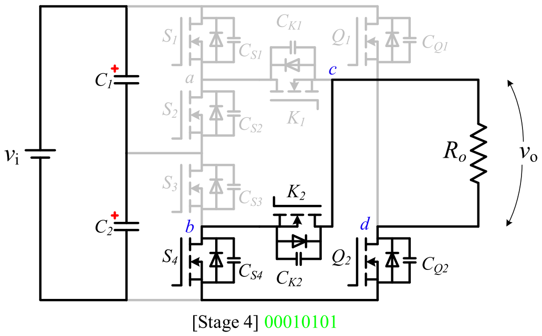

FIGURE 7. Equivalent circuits of [Stage 4].

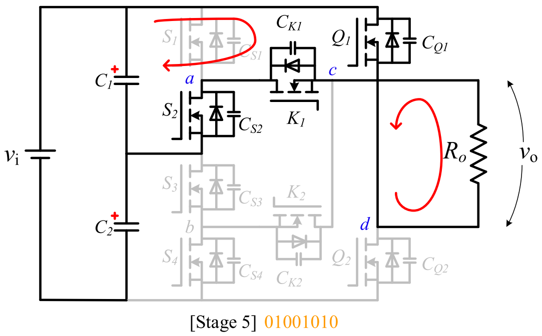

FIGURE 8. Equivalent circuits of [Stage 5].

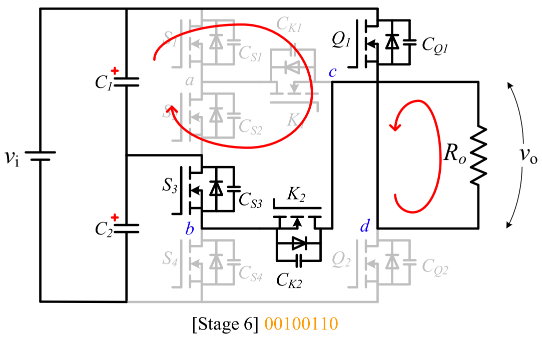

FIGURE 9. Equivalent circuits of [Stage 6].

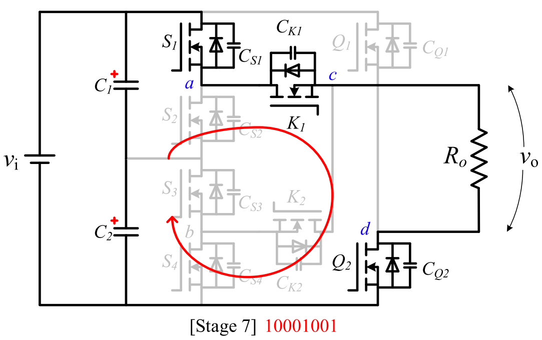

FIGURE 10. Equivalent circuits of [Stage 7].

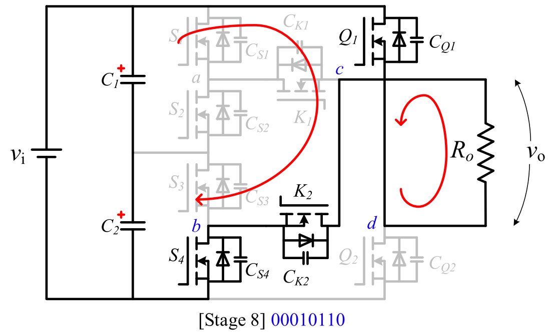

FIGURE 11. Equivalent circuits of [Stage 8].

[Stage 2] (00100101): While S_3, K_2 and Q_2 are conducting in this stage, input capacitor C_2 is connected to the load. Thus the output voltage is clamped to $v_i/2$. The input capacitor C_2 is discharged in this stage, while the input capacitor C_1 is charged by the input voltage source at the same time, as a result the voltage sum of C_1 and C_2 keeps the same. This working stage is nearly the same with [stage 1], the output voltage is also clamped by C_2, the only difference lies in the conducting switches.

[Stage 3] (10001010): While S_1, K_1 and Q_1 are conducting in this stage, the load is bypassed by the circuit. Thus the output voltage is clamped to zero voltage. The input capacitor C_1 and C_2 are charged by the input voltage source, and the voltage sum of C_1 and C_2 keeps the same.

[Stage 4] (00010101): While S_4, K_2 and Q_2 are conducting in this stage, the load is bypassed by the circuit. Thus the output voltage is clamped to zero voltage. The input capacitor C_1 and C_2 are charged by the input voltage source, and the voltage sum of C_1 and C_2 keeps the same. This working stage is nearly the same with [stage 3], the output voltage is also clamped to zero, the only difference lies in the conducting switches.

[Stage 5] (01001010): While S_2, K_1 and Q_1 are conducting in this stage, input capacitor C_1 is connected to the load inversely. Thus the output voltage is clamped to $-v_i/2$. The input capacitor C_1 is discharged in this stage, while the input capacitor C_2 is charged by the input voltage source at the same time, as a result the voltage sum of C_1 and C_2 keeps the same.

[Stage 6] (00100110): While S_3, K_2 and Q_1 are conducting in this stage, input capacitor C_1 is connected to the load inversely. Thus the output voltage is clamped to $-v_i/2$. The input capacitor C_1 is discharged in this stage, while the input capacitor C_2 is charged by the input voltage source at the same time, as a result the voltage sum of C_1 and C_2 keeps the same. This working stage is nearly the same with [stage 5], the output voltage is also clamped by C_1, the only difference lies in the conducting switches

[Stage 7] (10001001): While S_1, K_1 and Q_2 are conducting in this stage, input capacitor C_1 and C_2 are connected to the load in series. Thus the output voltage is clamped to v_i. The input capacitor C_1 and C_2 are discharged in this stage, while they are charged by the input voltage source at the same time, as a result the voltage sum of C_1 and C_2 keeps the same.

[Stage 8] (0010110): While S_4, K_2 and Q_1 are conducting in this stage, input capacitor C_1 and C_2 are connected to the load inversely. Thus the output voltage is clamped to $-v_i$. The input capacitor C_1 and C_2 are discharged in this stage, while they are charged by the input voltage source at the same time, as a result the voltage sum of C_1 and C_2 keeps the same.

IV. CONTROL AND OUTPUT ALGORITHM

A. OUTPUT STRATEGIES

Due to the voltage level selector, there are two output strategies with respected to the load condition. The first one is low frequency fitting strategy, and the next one is high frequency SPWM strategy

For low frequency fitting (LFF) strategy:

In this strategy, the switching frequency is the same with the frequency of the modulation wave. The key idea of this strategy is to find the closest value among the five voltage levels to fit the output wave while modulation wave changes. The algorithm is shown in Fig. 12.

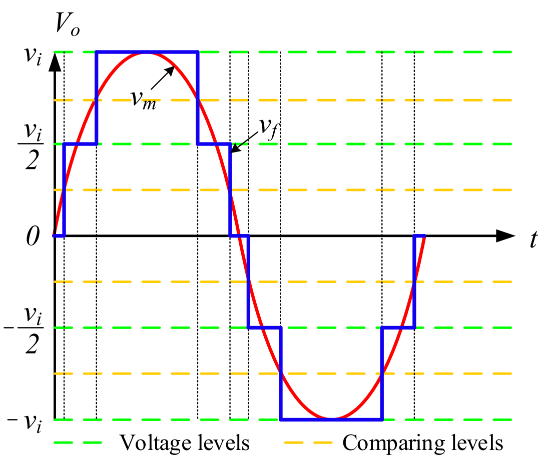

FIGURE 12. Illustration of the LFF output strategy.

As shown in Fig. 12, v_m is the modulation wave and v_f is the fitting wave. While v_m is a sinusoidal waveform, the value of v_f has only five options due to the configuration of the voltage selector. It is illustrated with green dotted lines in Fig. 12 and indicated in (1).

$$v_f = k\frac{v_i}{2}, \quad k = 0, \quad \pm 1, \quad \pm 2 \tag{1}$$

Thus, the key idea of this strategy is to find the optimized options and switching points to fit v_m in a low frequency condition. While v_m is affirmatory at any time, and only one best option exists among five voltage levels at any time. So the selector will choose the closest voltage level at each period, thus the switching points occur on the middle of each voltage levels. Switching points are given in (2) and the comparing lines are shown with brown lines in Fig. 12.

$$v_s = \frac{v_i}{4} + k\frac{v_i}{2}, \quad k = -2, -1, 0, 1 \tag{2}$$

Once v_m crosses the comparing lines, the work state and the output voltage level change. And the output voltage values with respect to v_m are indicated in (3).

$$v_s = \begin{cases} v_i, & v_m > \frac{3}{4}v_i \\ \frac{v_i}{2}, & \frac{1}{4}v_i < v_m < \frac{3}{4}v_i \\ 0, & -\frac{1}{4}v_i < v_m < \frac{1}{4}v_i \\ -\frac{v_i}{2}, & -\frac{3}{4}v_i < v_m < -\frac{1}{4}v_i \\ -v_i, & v_m < -\frac{3}{4}v_i \end{cases} \tag{3}$$

Thus the closest and optimized option of voltage selector is obtained, and with more cascaded cells which increases the voltage levels, v_f becomes more similar to v_m. The merit of this output strategy is that it works on a very low frequency. For less sensitive load conditions (ones don't have a strict limitation of high voltage quality, such as motor drive), low frequency strategy leads to lower switching losses.

For high frequency SPWM (HFSPWM) strategy:

While for sensitive load, which has a strict request on voltage quality, it is better to utilize the high frequency SPWM strategy to reduce THD (total harmonic distortion). The algorithm of this strategy is shown in Fig. 13.

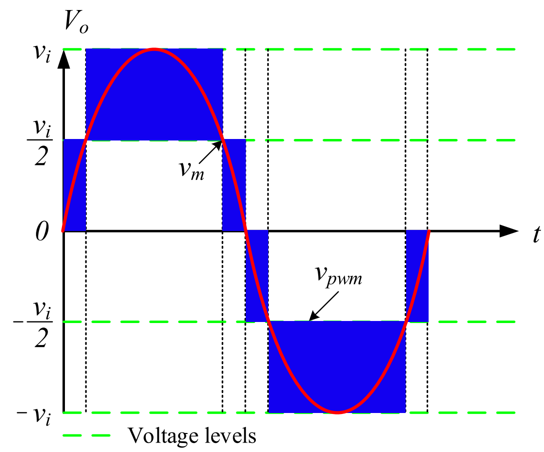

FIGURE 13. Illustration of the HFSPWM output strategy.

As shown in Fig. 13, the voltage levels are illustrated in green lines and the expression is the same with (1). v_m is the same modulation wave, and v_{spwm} is the SPWM wave. With the increasing of the switching frequency, it allows not only selecting one closest voltage level at each time, it allows to switch between two voltage levels in each time period. For example, when v_m is between 0 and $v_i/2$, the output voltage is switching between 0 and $v_i/2$ all the times with respect to the result of comparison. The higher switched level and the lower switched level are indicated in (4) and (5).

$$v_h = \begin{cases} v_i, & \frac{1}{2}v_i < v_m < v_i \\ \frac{v_i}{2}, & 0 < v_m < \frac{1}{2}v_i \\ 0, & -\frac{1}{2}v_i < v_m < 0 \\ -\frac{v_i}{2}, & -v_i < v_m < -\frac{1}{2}v_i \end{cases} \tag{4}$$

$$v_l = \begin{cases} \frac{v_i}{2}, & \frac{1}{2}v_i < v_m < v_i \\ 0, & 0 < v_m < \frac{1}{2}v_i \\ -\frac{1}{2}v_i, & -\frac{1}{2}v_i < v_m < 0 \\ -v_i, & -v_i < v_m < -\frac{1}{2}v_i \end{cases} \tag{5}$$

The algorithm of SPWM is shown in Fig. 14, v_{car} is the carrier wave which is a sawtooth wave in 5kHz. v_m' and v_{spwm}' are the equivalent modulation wave and SPWM wave in the same zone. v_h and v_l are the higher voltage level and lower voltage level indicated in (5), and the selection of v_{spwm}' between v_h and v_l in one carrier period is determined by the comparison result of v_m' and v_{car}.

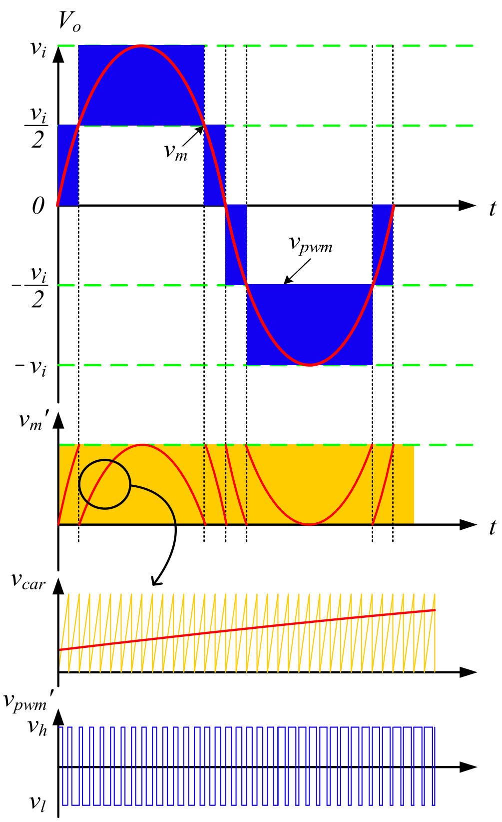

FIGURE 14. Illustration of the separated modulated wave in HFSPWM output strategy.

The high frequency strategy, which reduces the THD and improves the output voltage quality, is more suitable for strict load condition. However, there is a trade-off to choose between these two output strategies. LFF strategy for lower switching losses and HFSPWM strategy for lower THD losses and higher output voltage quality. Actually, hybrid output strategy is utilized to optimize the algorithm and reduce the total losses in practical engineering, thus improves the efficiency. And dynamic algorithm and detection are applied to switch between these two strategies.

B. VOLTAGE STRATEGY

The voltage balance strategy is applied to balance the voltage of the two input capacitors C_1 and C_2. C_1 discharges in stage 5-6 and C_2 discharges in stage 1-2. Thus it is convenient to balance the voltages through the adjustment of the discharging period of the two capacitors. The algorithm of the voltage balance strategy is shown in Fig. 15.

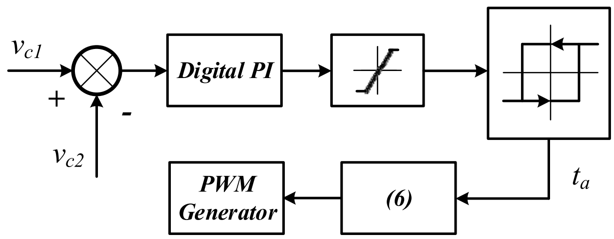

FIGURE 15. Algorithm of the voltage balance strategy.

As shown in Fig. 15, the voltage difference of C_1 and C_2 is detected and then sent to a PI module, after the amplitude limitation module and the hysteresis loop module, t_a is obtained. t_a is the adjusting time inserted to stage 1-2 and stage 5-6. It is indicated in (6).

$$\begin{cases} t'_{stage1} = t_{stage1} + t_a \\ t'_{stage2} = t_{stage2} + t_a \\ t'_{stage5} = t_{stage5} - t_a \\ t'_{stage6} = t_{stage6} - t_a \end{cases} \tag{6}$$

After the adjustment in time period, the SPWM generator will give the modified SPWM waveforms with changed discharging time for C_1 and C_2, and the voltages of them will be balanced.

C. SWITCHING OPTIMIZATION METHOD

To reduce the switching losses at fixed switching frequency as much as possible, an optimization method is adopted at stage switching time. The key thought of this method is to keep the least switches changed at each switching time. As shown in Fig. 4-11, there are 3 switches conducting on each stage, and the change between stages causes switching losses. The less switches changed, the lower switching losses caused. Fig. 16 shows the common switches between stages.

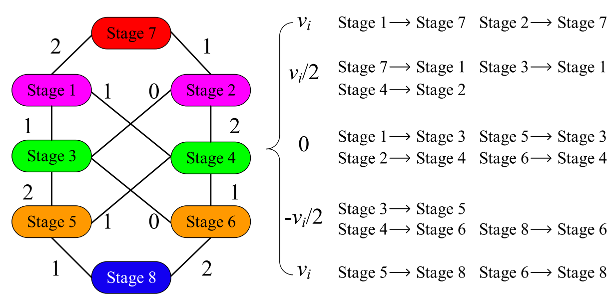

FIGURE 16. Diagram of common switches and optimization method.

As shown in Fig. 16, there are two stages for voltage level of $v_i/2$, 0 and $-v_i/2$. The optimization method is to determine which stage should be operated when these voltage levels should be outputted. Besides, only changes between contiguous voltage levels are allowed for continuous modulation waveform (for example change from stage 1 to stage 7 is allowed, but change from stage 1 to stage 2 or to stage 5 is not allowed). To make less conducting switches changed, the corresponding strategy is also illustrated in Fig. 16. As the next working stage is largely deal to the modulation waveform as well as the current working stage, it is necessary for the control unit to memorize the old working stage.

V. SIMULATION RESULTS

The simulation is carried out on PSIM, with time step $t_{step} = 10^{-6}$s. While the input source is a DC voltage source ($v_i = 20$V). The two input capacitors C_1 and C_2 are identical ($C_1 = C_2 = 6.8$mF). The eight switches are low voltage MOSFETs. And the load is represented by a resistor.

With low frequency fitting output strategy, the output waveforms are shown in Fig. 17. As shown in Fig. 17, v_o fits v_m well. And the switching frequency is very low, which is equal to the output frequency with respect to each switch.

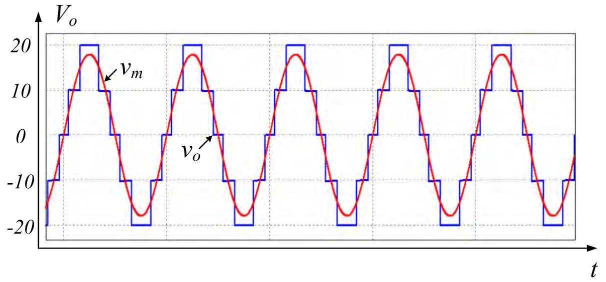

FIGURE 17. Waveforms with LFF strategy.

With high frequency SPWM output strategy, the output waveforms are shown in Fig. 18. As shown in Fig. 18, at each voltage zone, the output voltage v_o switches between v_h and v_l, which reduces the THD sharply. When voltage zone changes, v_h and v_l change automatically. With carrier wave of 5kHz, the SPWM wave is generated as shown in the figure.

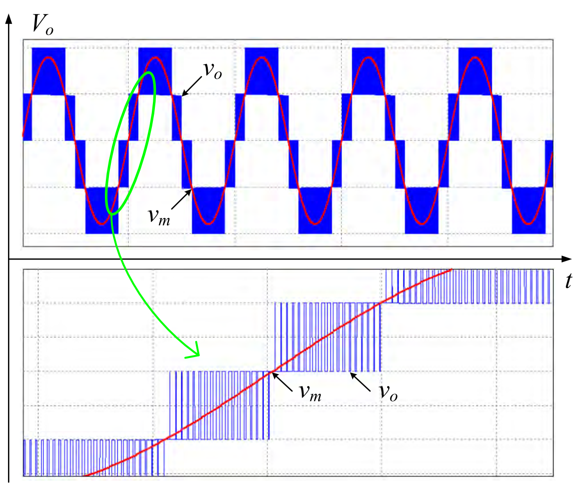

FIGURE 18. Waveforms with HFSPWM strategy.

The voltages of the input capacitors are shown in Fig. 19. As shown in Fig. 19, the voltages of the input capacitors are balanced. Little changes exist in each period, but the fluctuation is neglectable. Each working stage has its own charging and discharging characteristics on each capacitor. Time adjustment exists in stage 1-2 and stage 5-6 to balance the charging and discharging quantity, thus to balance the voltage. As a result, the voltage of each capacitor are nearly identical and constant in the whole simulation time.

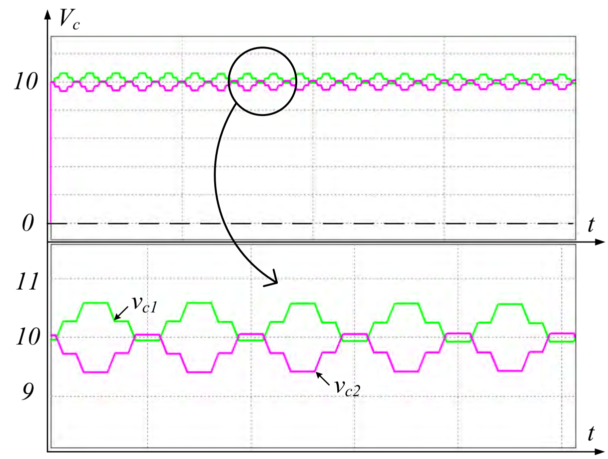

FIGURE 19. Voltages of input capacitors C_1 and C_2.

The proposed inverter has cascaded ability, and the simulation results of both output strategies with two cascaded inverter cells are given in Fig. 20. As shown in Fig. 20, 9-level output voltage is realized.

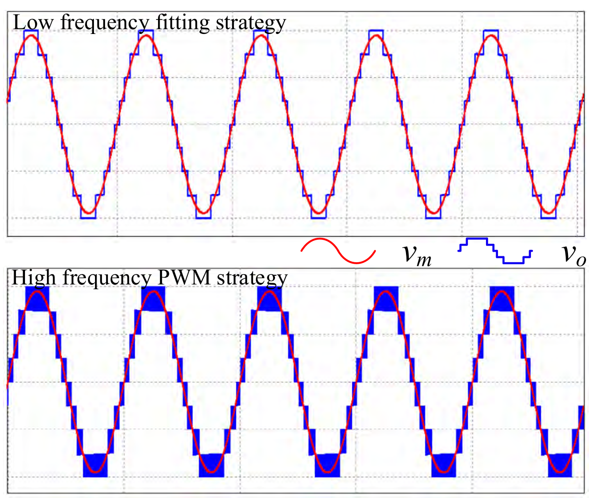

FIGURE 20. Output waveforms of 2-level cascaded topologies.

VI. LABORATORIAL EXPERIMENT

Based on the analysis above, an experimental prototype with 10V input voltage is built to verify the topology and test

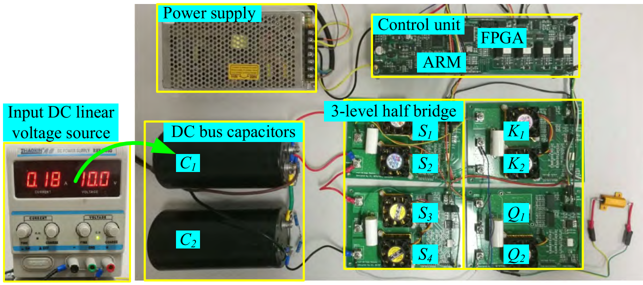

FIGURE 21. Experimental prototype of the proposed topology.

the efficiency. The prototype is shown in Fig. 21. The input voltage is supplied by adjustable linear voltage source (the voltage is set at 10V normally). While the eight switches are MOSFETs of IRF640N (a fan is implemented for each switch for cooling), the resistant load is 50Ω and the inductance load is 2mH. The DC bus capacitors are 6.8mF. The control unit consists of a FPGA chip for SPWM generation and an ARM chip to generate sinusoidal wave.

The output voltage of circuit point *a*, *b*, *c*, and *d* of both low and high frequency output strategies are shown in Fig. 22. As shown in Fig. 22, the voltages of the circuit points *a*, *b*, and *d* (described in the proposed topology and shown in Fig. 1 and Fig. 2) are 2-level, while the voltage of the circuit point *c* is 3-level. v_c is equal to v_a or v_b, determined by the voltage selector. Finally, the output voltage v_o is the difference between v_c and v_d ($v_o = v_c - v_d$). As shown in Fig. 22, v_d is always a square waveform in 50Hz. As v_d is key parameter which determines the sign (plus or minus) of the output voltage v_o, it should be in the same frequency with the modulated sinusoidal waveform in both output strategies.

The output voltage with two strategies of the multi-level inverter is shown in Fig. 23. As shown in Fig. 23, with low frequency fitting strategy, 5-level output is realized, and the switching frequency of each MOSFET is near to the modulation frequency (50Hz). With voltage balance strategy, voltages on the series connected DC bus capacitor are equal, as a result, the plus and minus $v_i/2$ voltage levels are exactly guaranteed. With high frequency SPWM strategy, the SPWM modulation is adopted at each voltage zones. As shown in Fig. 23, four voltage zones exist ($-v_i$ to $-v_i/2$, $-v_i/2$ to 0, 0 to $v_i/2$, and $v_i/2$ to v_i). And the output voltage are modulated between the upper and lower limitation of each voltage zone deal to the comparison of the carrier wave and modulated wave. While on the zone of $-v_i$ to $-v_i/2$ and $v_i/2$ to v_i, there is a period where only one output voltage level, which means the modulation wave is always larger (smaller) than the carrier wave as a condition of overload. On that condition, the inverter will output its largest (lowest) voltage to fit the voltage demand.

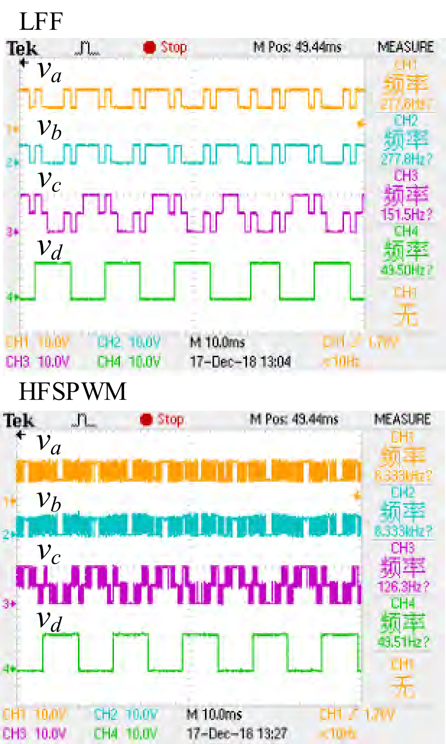

FIGURE 22. Circuit point voltages of the proposed topology.

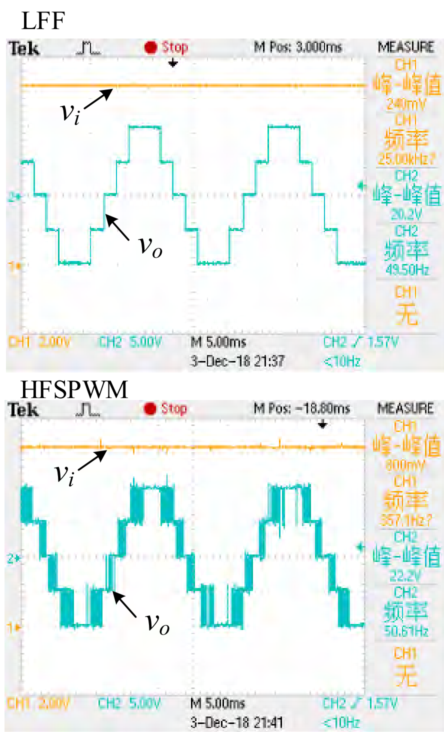

FIGURE 23. Input and output voltages of the proposed topology.

With inductance resistant load (50Ω and 2mH), the output voltage and output current (represented by the voltage of the resistor) are shown in Fig. 24. As shown in Fig. 24, the phase difference between output voltage and current is nearly zero with both strategies, which is mainly due to the low frequency fundamental sinusoidal wave (50Hz) and

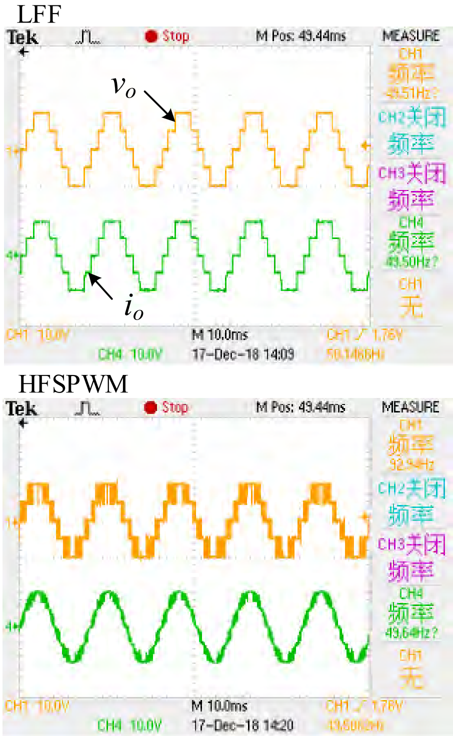

FIGURE 24. Output voltage and current of the proposed topology.

FIGURE 25. Comparison on THD losses of the proposed topology.

small inductor (2mH). But there is a difference of the filter effect of the current waveform between strategies. With the same inductor, the current waveform in low frequency strategy has less changed from resistant load. However, the current waveform in high frequency strategy has changed nearly to sinusoidal waveform. Which illustrates that the high frequency strategy has better output quality.

With the FFT function of the oscilloscope, the THD losses are obvious. The comparison of two strategies on THD are shown in Fig. 25. As shown in Fig. 25, the THD losses with high frequency SPWM strategy is much lower.

With the same configuration of the inverter, the efficiency of different input voltages are tested and the results are shown in Fig. 26. As shown in Fig. 26, on lower power conditions, the switching losses are obvious, thus low frequency fitting strategy has better performance on efficiency, while on higher power conditions, where harmonic losses dominate the efficiency, high frequency SPWM gets better performance.

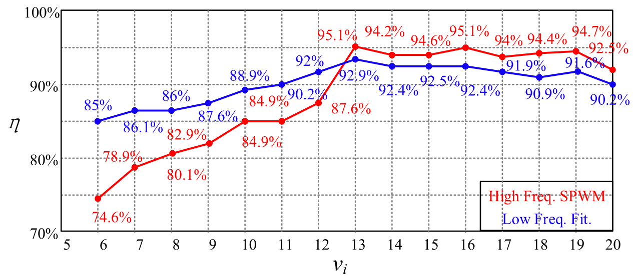

FIGURE 26. Efficiency with different input voltages.

VII. CONCLUSION

A novel multilevel inverter based on a three-level half bridge is proposed for DC/AC applications in this paper. For each power cell, only one DC power source is needed and 5-level output AC voltage is realized. Both positive and negative voltage levels are generated at the output, thus no extra H bridges are needed. The non-isolated topology (transformerless) eliminates magnetic losses. The operating principle and the working stages of the proposed inverter are introduced, while the two output strategies are discussed in detail. Besides, voltage balance strategy is adopted to balance the bus capacitor voltages, and stage optimization method is applied to further reduce the switching losses. Finally, a simulation is carried out to verify the two output strategies, voltage balance strategy and the cascaded ability, and a laboratorial experiment is carried out to test the THD losses and the total efficiency.

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CHAO ZHANG was born in Henan, China, in 1994. He received the B.S. degree in electrical engineering from the Beijing Institute of Technology, Beijing, China, in 2016, where he is currently pursuing the M.S. degree in electrical engineering.

His current research interests include cascaded H-bridge converters, DC-DC converters, and multilevel DC-AC converters.

ZHIGANG GAO was born in Hebei, China, in 1983. He received the B.S. degree from Tianjin University, Tianjin, China, in 2005, the M.S. degree in electrical engineering from the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, in 2008, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, in 2011.

In 2011, he joined the School of Automation, Beijing Institute of Technology, Beijing, where he is currently a Lecturer. His current research interests include power systems, multilevel converters, motor drives, and renewable resource generation.